Tests on the Relationship between the Oxide Thickness of CMOS Chips and

Their Resistance to Gamma Radiation

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Abstract

The tolerance level of selected commercial-off-the-shelf (COTS) CMOS devices to ionizing radiation was determined in a series of tests conducted at the University of Missouri – Rolla Nuclear Reactor facility. Care was taken as practical to follow the military standard, MIL-STD-883E during the test phase. The following CMOS AND gates were evaluated: ST Microelectronics M74HC08 (oxide thickness = 550 Å); Fairchild Semiconductor 74AC08 (250 Å); Texas Instruments SN74AHC08 (185 Å). The parameter most affected by ionizing radiation was the rise time. Rise time increased with increasing irradiation dose, especially in ICs with thick oxide layers. We estimate that the 550Å oxide ICs fail at frequencies higher than about 100 kHz after exposure to a dose of 10 MRad. Devices with thinner oxide layers remained operational at least at frequencies of 1 MHz even after irradiation with 16 MRad. Cost and time estimates of our testing procedure are discussed.

Keywords: CMOS, Oxide Thickness, Radiation Resistance, Gamma Radiation

I. Introduction

The current drive towards the use of commercial-off-the-shelf (COTS) semiconductor devices in space, avionic and (ionizing) radiation applications, even though the components are uncertified for such environments, poses the need for testing the radiation resistance (or equally the radiation tolerance) of COTS [1]. Here, we present a fast and inexpensive method to test the cumulative damage of gamma radiation on MOS-type COTS, and we apply the method to three commercially available CMOS AND gates.

In our method, ICs are exposed to gamma radiation by placing them in proximity of the fuel elements of a nuclear reactor after shutdown [2]. Radioactive isotopes produced during reactor operation generate dose rates of gamma rays which are comparable to the dose rates attainable with conventional gamma ray sources. With minor modifications to our procedure, irradiation and testing could be carried out according to MIL-STD-883E [3]. Compared to irradiation with more conventional gamma ray sources, our method decreases the risk for the operator, since the fuel rods are submerged in a water pool, which shields the gamma radiation. The method is also comparatively cheap, since irradiations can be carried out at times when the fuel rods are idle, such as during maintenance operations, or during temporary storage of spent fuel rods.

II. Experimental

A. Irradiation Procedure

Irradiation and testing procedures follow MIL-STD-883E, with the only exception that the time elapsed between irradiation and testing was not one hour, as required, but several hours. In principle, the time delay could be reduced to one hour as prescribed by the norms.

In a typical irradiation, the pool reactor at University of Missouri – Rolla (UMRR) was run at 180-200 kW for two hours. Irradiations started approximately one hour after shutdown. This is the minimum time necessary to let the neutron flux decay and prevent neutron activation of the ICs. ICs were inserted in a water-tight aluminum container, and placed in front of one fuel element inside the reactor cooling pool. Alternatively, ICs were placed in a plastic container and sent inside the reactor core with a pneumatic system (rabbit tube). All pins of the ICs were grounded during irradiation. In either case, typical initial dose rates were around 500 kRad/h at one hour after shutdown and decayed in a nearly exponential fashion to about 100 kRad/h, six hours after shutdown. Since most fission products are short-lived, the dose rate decayed exponentially, as shown in Fig. 1. For our experiments, we

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generally exposed ICs for typically one to two hours, which corresponds to a variation of about 50% of the dose rate, from a value of about 500 kRad/h to a value of 220 kRad/h.

Dose rate dependence of ICs irradiated with total high doses were determined by exposing ICs to a ⁶⁰Co source located at the Missouri University Research Reactor (MURR). This source allowed dose rates of up to 2.2 Mrad/h to be achieved. The dose rate can be varied by about a factor of 5 by placing the ICs at different distances from the source.





B. IC Test Procedure

Three types of CMOS AND gates from the same batch were selected to test. The main difference between the ICs was the oxide thickness, as shown in Table I.

Testing was carried out by connecting the chip's V_{CC} pin and one gate input to positive 5 volts, and a 0-5 volt square wave to the other input, while keeping all other pins grounded. The gate output was sent to an oscilloscope that measured the maximum output voltage and the rise time. This process was repeated for input frequencies from 100 to 1200 kHz.

Manufacturer	Part Number	Oxide Thickness (Å)
ST Microelectronics	M74HC08	550
Fairchild Semiconductor	74AC08	250
Texas Instruments	SN74AHC08	185

Table I. Types of CMOS AND gates used in experiments.

III. Results

Rise time and output voltage of each IC were measured before irradiation, and found to coincide within 5% for all ICs of the same model. The characteristics of ICs of the same type remained comparable in all ICs of the same type irradiated with the same total dose, independent of dose rate.

The dependence of rise time on frequency is shown in Fig. 2 for several total doses and for each oxide thickness. The rise time did not depend strongly on the testing frequency for all ICs. The dependence of rise time on irradiation dose is illustrated in Fig. 3 for a fixed input frequency of 1 MHz. The ICs with thinnest oxides (TI and Fairchild) did not show a strong dependence on irradiation dose. A strong dependence on total dose was exhibited by the IC with the thickest oxide layer (ST). This behavior is in accordance with previously reported data on MOS-type ICs exposed to gamma rays. Ionizing radiation generates electron-hole pairs in insulators. The electrons have a high mobility and they are generally swept out of the insulating layer. Holes are left behind, and are transported to the interfaces by electric fields. A fraction (20-40%) of the holes remains trapped at the interfaces, and their main effect is to shift the threshold voltage [4, 5]. Threshold voltage shifts, in turn, cause a series of problems, and affect mostly the response time of ICs [6]. Thin oxide layers are less affected than thick layers, since the amount of energy deposited by ionizing radiation is proportional to the oxide thickness [7, 8].

The output voltage was nearly independent of irradiation dose and testing frequency, as shown in Figs. 4 and 5. Variations were mostly due to the uncertainty of the input voltage, which was typically constant within ± 0.05 V.

IV. Conclusions

We present here a simple method to evaluate cumulative effects in CMOS devices induced by gamma radiation. The method is simple, can be adapted to follow MIL-STD-883E, is low cost (~\$200-250/hr) and is fast (~3-5 weeks). CMOS AND gates were evaluated, and their sensitivity to ionizing radiation was found to be strongly dependent on gate oxide thickness. The data indicates that for thicker oxide thicknesses the rise time will become the governing factor at lower frequencies. Failure for the 550Å oxide thickness is due to longer rise times beginning at frequencies around 100 kHz and higher. Around this point, as the rise time increases, the voltage will not reach full value before the gate turns back off. On the other hand, devices with thinner oxide layers should remain operational at least at frequencies of 1 MHz, even after irradiation with 16 MRad.



Fig. 2. Rise time dependence on input frequency and total ionization dose for ICs of different oxide thickness.

Fig. 3. Rise time dependence on total ionization dose for a fixed input frequency of 1 MHz.



Fig. 4. Output voltage dependence on input frequency for ICs of different oxide thickness.

Fig. 5. Output voltage dependence on total gamma-ray dose for a fixed input frequency of 1 MHz.

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